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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,816	02/27/2004	Hiroshi Suzuki	09856/0200497-US0	7981
7278	7590	05/26/2005	EXAMINER	
DARBY & DARBY P.C. P. O. BOX 5257 NEW YORK, NY 10150-5257			RILEY, SHAWN	
			ART UNIT	PAPER NUMBER

2838

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/788,816

Applicant(s)

SUZUKI, HIROSHI



Examiner

Shawn Riley

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date sep04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Objections

1. Claims 9, 10, 13, 14 objected to under 37 C.F.R. 1.75(a) because of the following informalities: for examination purposes, it is assumed that the preamble of these claims is referring to the method as opposed to the apparatus as currently recited. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. §102(b) as being fully anticipated by Dishner (U.S. Patent 4,801,859). Dishner shows,¹ (in, e.g., the(ir) figures and corresponding disclosure)

¹ Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material

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What is claimed is:

As to claim 1;

In a booster circuit (see, e.g., figures 3 and 4/5) wherein energy is stored in an inductor (L1) when a switching element (Q1) is on and said energy is superposed onto an input voltage (at 50) to charge a capacitor (C1, e.g., column 5 lines 45-50) disposed at an output side when said switching element is off, a booster circuit comprising: detecting means (SWITCH CONTROL CIRCUIT) detecting said input voltage (at 54) and an actual booster voltage (VC1) on said capacitor side; target booster setting means setting a target booster voltage (for example, 93 in figure 4); duty ratio setting means (in part including PWM Comparator) setting a duty ratio so that deviation between said target booster voltage and said actual booster voltage is eliminated; and controlling means (including 96/97/98) calculating a correction value based on an input voltage change obtained from said input voltage, correcting said duty ratio with said correction value, and performing feedback control based on said corrected duty ratio by turning said switching element on and off.

As to claim 2;

A booster circuit as described in claim 1 wherein said correction value is a ratio between an input voltage change calculated from said input voltage (VC2) and said target booster voltage (based on VREF1).

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As to claim 3;

A booster circuit as described in claim 1 wherein said correction value is a ratio between an input voltage change calculated from said input voltage (at VC2 at 54) and said actual booster voltage (at VC1 at 50).

For method claims 4-6, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986).

Therefore the previous rejections based on the apparatus will not be repeated.

4. In a method for controlling a booster circuit wherein energy is stored in an inductor when a switching element is on and said energy is superposed onto an input voltage to charge a capacitor disposed at an output side when said switching element is off, a method for controlling a booster circuit comprising: detecting said input voltage and an actual booster voltage on said capacitor side; setting a target booster voltage; setting a duty ratio to eliminate a deviation between said target booster voltage and said actual booster voltage; calculating a correction value based on an input voltage change obtained from said input voltage; and performing feedback control by turning on and off said switching element based on a new duty ratio formed by correcting said duty ratio with said correction value.

5. A method for controlling a booster circuit as described in claim 4 wherein said correction value is a ratio between said input voltage change calculated based on said input voltage and said target booster voltage.

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6. A method for controlling a booster circuit as described in claim 4 wherein said correction value is a ratio between said input voltage change calculated based on said input voltage and said actual booster voltage.

As to claim 7;

A booster circuit as described in claim 2 wherein said controlling means comprises a correcting means (controlling means include 96/97/98) for calculating said correction value.

As to claim 8;

A booster circuit as described in claim 7 wherein said correcting means is a booster control module (correcting means is part of the booster circuit and therefore a booster control module).

As to claim 9;

A booster circuit as described in claim 5 wherein said controlling means comprises a correcting means (controlling means include 96/97/98) for calculating said correction value.

As to claim 10;

A booster circuit as described in claim 9 wherein said correcting means is a booster control module (the correcting means is part of the booster circuit and therefore a booster control module).

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As to claim 11;

A booster circuit as described in claim 3 wherein said controlling means comprises a correcting means (controlling means include 96/97/98) for calculating said correction value.

As to claim 12;

A booster circuit as described in claim 11 wherein said correcting means is a booster control module (the correcting means is part of the booster circuit and therefore a booster control module).

As to claim 13;

A booster circuit as described in claim 6 wherein said controlling means comprises a correcting means (controlling means include 96/97/98) for calculating said correction value.

As to claim 14;

A booster circuit as described in claim 13 wherein said correcting means is a booster control module (the correcting means is part of the booster circuit and therefore a booster control module).

Allowable Subject Matter


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3. No claims are allowable over the prior art of record.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at <http://pair-direct.uspto.gov> wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

May 05



Shawn Riley
Primary Examiner